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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/618,933 | 07/14/2003 | Marcos Karnezos | CPAC 1041-2 | 6636 |

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| EXAMINER | |
|---|---|
| CHAMBLISS, ALONZO | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2814 | |

DATE MAILED: 03/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/618,933 | KARNEZOS, MARCOS | |
| | Examiner | Art Unit | |
| | Alonzo Chambliss | 2814 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *04 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-58* is/are pending in the application.

4a) Of the above claim(s) *4,5,9,14,22-24,32,33,35,37,46-48 and 56-58* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-8,10-13,15,16,25,27,29-31,34,36,38-40,49,50,52,54 and 55* is/are rejected.

7)☒ Claim(s) *17-21,26,28,41-45,51 and 53* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *3/3/05*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election of claims 1-3, 6, 8, 10-13, 15-21, 25-28, 29-31, 34, 36, 38-45, and 49-55 in the reply filed on 1/4/05 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

2. Claims 4, 5, 9, 14, 22-24, 32, 33, 35, 37, and 46-48 withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Claims 56-58 have been withdrawn based on an election filed on 7/28/04.

### *Information Disclosure Statement*

3. The information disclosure statement (IDS) submitted on 12/29/03 was filed before the mailing date of the non-final rejection on 3/5/05. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

### *Drawings*

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 721 and 817. Also, the drawings are objected to because they do not include the following reference sign(s) mentioned in the description: 100'. Corrected

drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

5. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the first package that is a LGA package, wherein the memory package stack comprises a first package affixed onto a firs surface of a package stack substrate and a second package affixed onto a second surface of the package stack substrate must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate

changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Rejections - 35 USC § 102*

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-3, 8, 11-13, 15, 16, 29-31, 36, 39, 40, 54, and 55 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Watanabe et al. (US 4,982,265).

With respect to Claims 1, 11-13, and 29, Watanabe teaches a module substrate 271, a processor 3 (i.e. decoder) mounted on a portion of a first surface of the module substrate 271, and a plurality of memory package stack (i.e. the combination of 4A, 5A, 7 is the first package and 4B, 5B, 7 is the second package) (i.e. RAM) disposed over a portion of the module substrate 271 adjacent the portion to which the processor 3 is mounted (see col. 5 lines 40-68; Figs. 1-5 and 38).

With respect to Claims 2 and 30, Watanabe teaches wherein the processor is mounted onto a portion of the module substrate surface about the center, and wherein the memory package stack is disposed in part over a portion of the module substrate surface partly to one side of the portion to which the processor is mounted (see Figs. 1-5).

With respect to Claims 3 and 31, Watanabe teaches wherein the memory package stack is mounted onto a portion of the module substrate adjacent the portion to which the processor is mounted (see Figs. 1-5).

With respect to Claims 8, 15, 36, 39, Watanabe teaches wherein the memory package stack comprises a first package affixed onto a first surface of a package stack substrate 1 and a second package affixed onto a second surface of the package stack substrate 1 (see Figs. 1-5 and 38).

With respect to Claims 16 and 40, Watanabe teaches wherein the plurality of memory package stacks comprise a memory package assembly, and wherein a common memory package assembly substrate 1 comprises the package stack substrate for each of the plurality of the memory package stacks (see Figs. 1-5 and 38).

With respect to Claims 54 and 55, Watanabe teaches two of the memory package stacks, one each disposed on opposite sides of the processor (see Figs. 1-5).

8. Claims 1-3, 8, 11-13, 15, 16, 29-31, 36, 39, 40, 54, and 55 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Stoller (US 6,392,896).

With respect to Claims 1, 11-13, and 29, Stoller teaches a module substrate 29, a processor 30 (i.e. logic device or ASIC) mounted on a portion of a first surface of the

module substrate 29, and a plurality of memory package stack 12 disposed over a portion of the module substrate 29 adjacent the portion to which the processor 3 is mounted (see col. 3 lines 22-66 and col. 4 lines 1-67; Figs. 1-4, 6A, and 6B).

With respect to Claims 2 and 30, Stoller teaches wherein the processor is mounted onto a portion of the module substrate surface about the center, and wherein the memory package stack is disposed in part over a portion of the module substrate surface partly to one side of the portion to which the processor is mounted (see Figs. 1-4, 6A, and 6B).

With respect to Claims 3 and 31, Stroller teaches wherein the memory package stack is mounted onto a portion of the module substrate adjacent the portion to which the processor is mounted (see Figs. 1-4, 6A, and 6B).

With respect to Claims 8, 15, 36, 39, Stroller teaches wherein the memory package stack comprises a first package affixed onto a first surface of a package stack substrate 14 and a second package affixed onto a second surface of the package stack substrate 14 (see Figs. 1-4, 6A, and 6B).

With respect to Claims 16 and 40, Watanabe teaches wherein the plurality of memory package stacks comprise a memory package assembly, and wherein a common memory package assembly substrate 14 comprises the package stack substrate for each of the plurality of the memory package stacks (see Figs. 1-4, 6A, and 6B).

With respect to Claims 54 and 55, Watanabe teaches two of the memory package stacks, one each disposed on opposite sides of the processor (see Figs. 1-4, 6A, and 6B).

9. Claims 1-3, 11-13, 29-31, 54, and 55 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Streltsov (US 6,829,147).

With respect to Claims 1, 11-13, and 29, Streltsov teaches a module substrate 1, a processor 2 mounted on a portion of a first surface of the module substrate , and a plurality of memory package stack 3 disposed over a portion of the module substrate 1 adjacent the portion to which the processor 2 is mounted (see col. 2 lines 1-67; Fig. 1).

With respect to Claims 2 and 30, Streltsov teaches wherein the processor is mounted onto a portion of the module substrate surface about the center, and wherein the memory package stack is disposed in part over a portion of the module substrate surface partly to one side of the portion to which the processor is mounted (see Fig. 1).

With respect to Claims 3 and 31, Streltsov teaches wherein the memory package stack is mounted onto a portion of the module substrate adjacent the portion to which the processor is mounted (see Fig. 1).

With respect to Claims 54 and 55, Streltsov teaches two of the memory package stacks, one each disposed on opposite sides of the processor (see Fig. 1).

***Claim Rejections - 35 USC § 103***

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 6, 10, 34, 38, 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. (US 4,982,265) as applied to claims 1, 8, 29, and 36 above, and further in view of Michael (US 6,778,390) and Huang et al. (U.S. 6,495,912).

With respect to Claims 6 and 34, Watanabe fails to explicitly disclose the processor that comprises a GPU. However, it is well known in the semiconductor industry that a processor can be GPU as evident by Michael (see col. 2 lines 11-14).

With respect to Claims 10, 38, and 49, Watanabe discloses the claimed invention except for the first package that is a LGA package. However, Huang discloses that it is well known in the semiconductor industry to substitute a LGA for a TAB configuration (see col. 1 lines 33-48). Therefore, one skilled in the art at the time of invention would readily recognize substituting a LGA configuration for a TAB configuration of Watanabe, since the LGA configuration provides a reliable approach for electrical connected semiconductor packages as taught by Huang.

With respect to Claims 25, 27, 50, and 52, based on the configuration of the LGA package taught by Huang, the result would create each LGA memory package in the stack that is electrically connected to the memory stack substrate by wire bonding, and a z-interconnection between the LGA memory packages and the module substrate is made by wire bonding between each LGA memory package substrate and the module substrate.

12. Claim 6, 10, 34, and 38, 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stoller (US 6,392,896) as applied to claim 1, 8, 29, and 36 above, and further in view of Michael (US 6,778,390) and Huang et al. (U.S. 6,495,912).

With respect to Claims 6 and 34, Stoller fails to explicitly disclose the processor that comprises a GPU. However, it is well known in the semiconductor industry that a processor can be GPU as evident by Michael (see col. 2 lines 11-14).

With respect to Claims 10, 38, and 49, Stoller discloses the claimed invention except for the first package that is a LGA package. However, Huang discloses that it is well known in the semiconductor industry to substitute a LGA for a BGA configuration (see col. 1 lines 33-48). Therefore, one skilled in the art at the time of invention would readily recognize substituting a LGA configuration for a BGA configuration of Stoller, since the LGA configuration provides a reliable approach for electrical connected semiconductor packages as taught by Huang.

With respect to Claims 25, 27, 50, and 52, based on the configuration of the LGA package taught by Huang, the result would create each LGA memory package in the stack that is electrically connected to the memory stack substrate by wire bonding, and a z-interconnection between the LGA memory packages and the module substrate is made by wire bonding between each LGA memory package substrate and the module substrate.

***Allowable Subject Matter***

13. Claim 17-21, 26, 28, 41-45, 51, and 53 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowance subject matter: the prior art of record does not teach or suggest the combination of wherein the common memory assembly substrate spans the portion of the module substrate onto which the processor is mounted in claims 17 and 41.

A LGA memory packages in the stack are stacked in like orientation, and are separated by spacers to provide relief for z-interconnect wire bond loops between a lower package in the stack and the module substrate in claims 26 and 51.

A lower LGA package is affixed to and is wire bond connected to a lower surface of the common memory assembly substrate and an upper LGA package is inverted and affixed to and is wire bond connected to an upper surface of the common memory assembly substrate in claims 28 and 53.

The prior art made of record and not relied upon is cited primarily to show the product of the instant invention.

**Conclusion**

14. Any inquiry concerning the communication or earlier communications from the examiner should be directed to Alonzo Chambliss whose telephone number is (571) 272-1927.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-7956

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system Status information for published applications may be obtained from either Private PMR or Public PMR. Status information for unpublished applications is available through Private PMR only. For more information about the PMR system see http://pair-dkect.uspto.gov. Should you have questions on access to the Private PMR system contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC_Support@uspto.gov.

Alonzo Chambliss
Primary Patent Examiner
Art Unit 2814

**AC**/March 5, 2005